II Year II Semester	**L**	**T**	**P**	**C**
Code: 20EC4748	**3**	**1**	**0**	**4**

DIGITAL LOGIC FAMILIES

Course Objectives:

1. To learn various digital design methodologies and constraints
2. To realize logic gates using diode logic and transistor logic.
3. To relate logic levels, noise margins and design logic gates using TTL
4. To study the characteristics of differential amplifier and design logic gates using ECL
5. To describe electrical behavior of CMOS and design logic gates using CMOS

UNIT – I: **Digital Design**

About Digital Design, Analog versus Digital, Digital devices, Electronic Aspects of Digital Design, Software Aspects of Digital Design, Integrated circuits, Programmable Logic Devices, Application Specific IC's, Printed Circuit Boards, Digital–Design Levels, The Name of the Game.

UNIT–II: Diode Logic and Transistor Logic

Introduction to logic families, Types of Logic families, Logic gates – AND, OR, NOT, NAND, NOR, XOR, XNOR, AOI, OAI realization using truth table. Diode switching action, Transistor as a switch, Schottky Diodes and Transistors. Logic Levels, Noise Margins, Characteristics and Logic Gates realization using Diode Logic, Transistor Logic, Diode-Transistor Logic.

UNIT–III: Transistor-Transistor Logic

TTL Logic Levels, Noise Margins, TTL Characteristics, TTL Inverter/Buffer Circuit, TTLNAND/AND Circuit, TTL NOR/OR Circuit, Fan-in and Fan-out, Design considerations of TTL, TTL Families.

UNIT–IV: ECL Logic

ECL Logic Levels, Noise Margins, Basic Concept of a Differential Amplifier, ECL Characteristics, ECL Inverter/Buffer Circuit, ECL NAND/AND Circuit, ECL NOR/OR Circuit, Design considerations of ECL, Positive ECL, ECL10K/10H Families, ECL 100KFamily.

UNIT–V: CMOS Logic

CMOS Logic Levels, Noise Margins, MOS Transistors, Basic CMOS Inverter Circuit, CMOS NAND and NOR gates, Non-inverting Gates, CMOS AND-OR-INVERT and OR-AND-INVERT Gates, CMOS Steady State Electrical Behaviour, Fan-in and Fan-out, CMOS Dynamic Electrical Behaviour, CMOS Logic Families.

Course Outcomes:

A student who successfully fulfils this course requirement will be able to:

S.No	Course Outcome	BTL
1.	Summarize the fundamentals of digital design, different forms of digital devices and their constraints.	L2
2.	Classify the logic families and design logic circuits using diodes and transistors.	L5
3.	Relate the logic levels, noise margins and design logic circuits using TTL.	L5
4.	Explain ECL logic families and design logic circuits using ECL	L5
5.	Design and analyse CMOS logic families.	L5

Correlation of COs with POs& PSOs:

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	-	-	-	-	-	-	-	-	-	-	-	1	-
CO2	3	1	2	-	-	-	-	-	-	-	-	-	2	-
CO3	2	1	2	-	-	-	-	-	-	-	-	-	2	-
CO4	2	1	2	-	-	-	-	-	-	-	-	-	2	-
CO5	2	2	2	-	-	-	-	-	-	-	-	1	3	-

Text Books:

1. Digital Design Principles &Practices – John F. Wakerly, PHI/ Pearson Education, Third Edition, 2005.
2. CMOS Digital IC Circuit Analysis & Design – Kang &Leblebigi, McGraw Hill, 2003.
3. Pulse and Digital Circuits – A. Anand Kumar, Prentice Hall of India, Second Edition.

Reference Books:

1. Fundamentals of Digital Logic with VHDL Design – Stephen Brown & Zvonko Vranesic, McGraw Hill, Third Edition.
2. Digital Integrated Circuits Design – Rabey, Pearson Education, Second Edition, 2003.