II Year I Semester	**L**	**T**	**P**	**C**
Code: 20EC3002	**3**	**0**	**0**	**3**

DIGITAL ELECTRONICS

Course Objectives:

1. To understand the binary number system & codes and various Boolean theorems to perform logical operations.
2. To learn the minimization techniques and design gate level combinational logic circuits
3. To realize combinational logic circuits for ICs and understand the basics of PLDs
4. To classify and design sequential logic circuits
5. To categorize and analyse various Finite State Machines

UNIT–I Review of Number Systems & Boolean Theorems

Review of Number Systems: Representation of numbers of different radix, conversation from one radix to another radix, r–1'scompliments and r's compliments of signed members, floating point representation, Gray code,4-bit codes – BCD, Excess-3,2421, 84-2-1 code etc., Error detection & correction codes – parity checking, even parity, odd parity, hamming code.

Boolean Theorems and Logic Operations: Boolean theorems, principle of complementation & duality, De-Morgan theorems. Logic operations; Basic logic operations – NOT, OR, AND, Universal Logic operations, EX-OR, EX-NOR operations, Standard SOP and POS Forms, NAND-NAND and NOR-NOR realizations, Realization of three level logic circuits. Study the pin diagram and obtain truth table for thefollowingrelevantICs7400, 7402, 7404,7408,7432,7486.

UNIT–II Minimization Techniques & Combinational Logic circuit Designs

Minimization Techniques: Minimization and realization of switching functions using Boolean theorems, K-Map (up to 6variables) and tabular method (Quine-McCluskey method) with only four variables and single function.

Combinational Logic circuit Designs: Design of half adder, full adder, half subtractor, full subtractor, applications of full adders; 4-bitadder-subtractor circuit, BCD adder circuit, Excess 3 adder circuit and carry look-a-head adder, Carry select adder, Design code converts using Karnaugh method and draw the complete circuit diagrams.

UNIT–III Combinational Logic Circuits using LSI & MSI

Design of encoder, decoder, multiplexer and de-multiplexers, Implementation of higher order circuits using lower order circuits. Realization of Boolean functions using decoders and multiplexers. Design of Priority encoder, 4-bit digital comparator and seven segment decoder Study the relevant ICs pin diagrams and their functions 7442, 7447, 7485, 74154. Introduction to PLDs: PROM, PAL, PLA -Basics structures, realization of Boolean functions, Programming table.

UNIT–IV: Sequential Circuits - I

Classification of sequential circuits (synchronous and asynchronous), operation of NAND &NOR latches and flip-flops; truth tables and excitation tables of RS flip-flop, JK flip-flop, Tflip-flop, D flip-flop with preset and clear terminals, Master-slave JK Flip-flop, Conversion from one flip-flop to another flip-flop. Design of registers - Buffer register, control buffer register, shift register, bi-directional shift register, universal shift register. Design of ripple

counters, design of synchronous counters, Johnson counter, ring counter, Mod-N counter. Study the following relevant ICs and their relevant functions 7474, 7475, 7476, 7490, 7493, 74121.

UNIT–V: Sequential Circuits - II

Finite state machine; state diagrams, state tables, reduction of state tables. Analysis of clocked sequential circuits Mealy to Moore conversion and vice-versa. Realization of sequence generator, Design of Clocked Sequential Circuit to detect the given sequence (with overlapping or without overlapping). Real time example: Vending machine, Traffic light controller.

Course Outcomes:

A student who successfully fulfils this course requirement will be able to:

S.No	Course Outcome	BTL
1.	Understand number base conversions, Boolean algebra theorems, logic circuits behaviour and error coding techniques	L2
2.	Realize and design combinational logic circuits using minimization techniques	L5
3.	Design and analyse various combinational logic circuits using ICs and define PLDs	L5
4.	Categorize and design sequential logic circuits	L5
5.	Classify, design and analyse Finite State Machines	L5

Correlation of COs with POs& PSOs:

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	2	1	-	-	-	-	-	-	-	-	-	2	-
CO2	2	3	2	-	-	-	-	-	-	-	-	-	3	-
CO3	2	3	2	-	-	-	-	-	-	-	-	-	3	-
CO4	2	3	2	-	-	-	-	-	-	-	-	-	3	-
CO5	2	3	2	1	-	-	-	-	-	-	-	-	3	-

Text Books:

1. Digital Design–M. Morris Mano & Michael D.Ciletti, Prentice Hall of India, Fourth Edition, 2008.
2. Switching and Finite Automata Theory– Zvi Kohavi, Niraj K.Jha, Cambridge University Press, Third Edition, 2009.
3. Switching Theory and Logic Design– Hilland Peterson, John Wiley, Second Edition, 2012.

Reference Books:

1. Fundamentals of Logic Design–Charles H.Roth Jr, Jaico Publishers, 2006.
2. Digital Electronics–RS Sedha, S.Chand & company limited, 2010.
3. Switching Theory and Logic Design– A. Anand Kumar, Prentice Hall of India, 2016.
4. TTL74-Seriesdatabook.